Registration No.: | | | | | | | | | | |

Total Number of Pages: 02

Course: B.Tech/IDD
Sub_Code: EOPC2002

3rd Semester Regular/Back Examination: 2025-26
SUBJECT: Analog and Digital Electronic Circuits
BRANCH(S): EE, BIOMED, EEE, ELECTRICAL, ELECTRICAL & C.E, ELECTRONICS & C. E
Time: 3 Hours
Max Marks: 100
Q.Code: U558

Answer Q1 (Part-I) which is compulsory, any eight from Part-II, and any two from Part-III.
The figures in the right-hand margin indicate marks.

Part-I

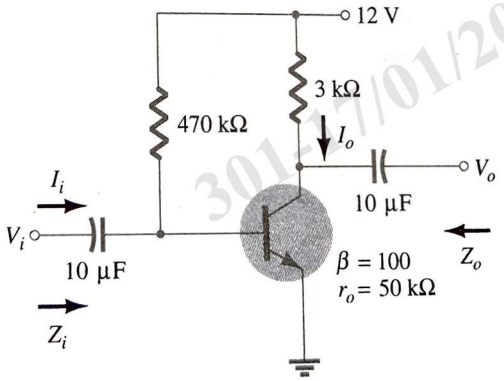
Q1 **Answer the following questions:** **(2 x 10)**

a) What is load line? Why this is straight line?
b) What is a model? Obtain the r_e model of all the three configurations of BJT.
c) Draw and explain the fixed bias configuration using a P-channel depletion type MOSFET.
d) Draw the equivalent model of JFET voltage divider configuration and find its Z_i and Z_o.
e) Explain the Wien-Bridge oscillator circuit.
f) How class B amplifier is different from class A amplifier?
g) Simplify the Boolean expression $Y = \sum m\,(2, 4, 6)$.
h) Derive the K-maps and simplified expressions for outputs of a half adder.
i) Differentiate between a combinational circuit and a sequential circuit.
j) How registers are designed? How can you classify registers? Explain.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

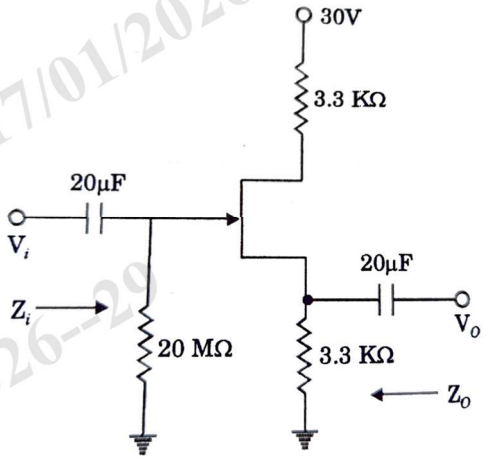
a) Explain the operation of voltage divider biasing using BJT. Why is it widely used?
b) For the network of figure given below,
I) Find Z_i, Z_o, A_v, and A_i with $r_e = \infty$.
II) Repeat (I) with $r_e = 50\ \Omega$.



c) For a voltage feedback biasing circuit with β = 45, V_{CC} = 24 V, V_{CE} = 5 V, R_C = 10 KΩ, and R_E = 270 Ω, find the value of feedback resistance R.
d) Explain the self-bias configuration of FET biasing. Discuss about its stability.

e) Draw the small signal equivalent model of a common source amplifier circuit using N-Channel D-MOSFET and find its necessary parameters Z_i, Z_o, A_v, and A_i

f) Determine the value of Z_i, Z_o, A_v, and A_i for the given circuit with I_{DSS} = 6 mA, V_P = 6 V, and R_d = 40 KΩ



g) Write the Bark-Hausen's criteria for oscillation. Explain the working principle of an oscillator.

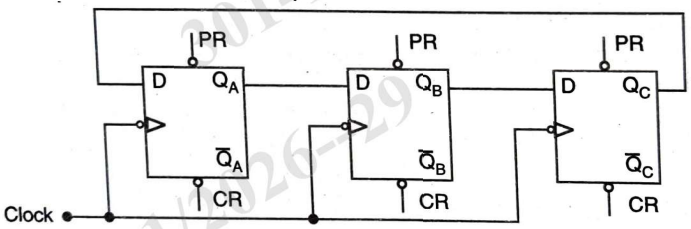
h) Explain the RC-Phase shift oscillator and find the expression for the frequency of oscillation.

i) Use the Quine-McCluskey method of minimization and find the expression for
$f(A, B, C, D) = \sum m(2, 4, 8, 11, 15) + d(1, 10, 12, 13)$

j) Implement a full adder using 8:1 multiplexer.

k) Explain the working operation of a D-flip flop.

l) Consider the given circuit shown below. Here the initial output condition is $Q_AQ_BQ_C$ = 010. Write the truth table of output $Q_AQ_BQ_C$ for 4 clock pulses.



Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Discuss all about the compound configurations of cascade, cascode, Darlington, and current mirror circuits **(16)**

Q4 Find the parameters Z_i, Z_o, A_v, and A_i of Common gate and source follower amplifiers. **(16)**

Q5 What is a power amplifier? How is it classified? Explain the operation of push-pull amplifier circuit. Find the efficiency of class-B amplifier and compare it with that of class-A amplifier **(16)**

Q6 Write a note on one bit magnitude comparator. Design a ripple counter for the state diagram shown in figure below. **(16)**