Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech**
RCS4D001

6th Semester Regular/Back Examination: 2024-25
SUBJECT: Computer Organisation and Architecture
BRANCH(S): EEE, ELECTRICAL
Time: 3 Hours
Max Marks: 100
Q.Code: S029

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) List the main functional blocks of a computer.
b) Mention two commonly used cache replacement algorithms.
c) Explain any two addressing modes used by CPUs.
d) What is RTL (Register Transfer Language) interpretation of instructions?
e) Describe signed number representation in computing.
f) What is ripple carry adder?
g) Explain briefly what software interrupts are.
h) Define memory interleaving.
i) What is DMA (Direct Memory Access)?
j) Define privileged and non-privileged instructions.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Describe the instruction execution cycle with an example.
b) Compare and contrast fixed and floating-point number representations.
c) Explain Booth's multiplication algorithm with an illustrative example.
d) Discuss restoring and non-restoring division techniques with suitable examples.
e) Describe the architecture and features of x86 processors briefly.
f) Outline the differences between hardwired and micro-programmed CPU designs.
g) Explain the roles and functioning of interrupt-driven I/O.
h) Discuss how interrupts affect process state transitions.
i) Explain hierarchical memory organization with a suitable diagram.
j) Illustrate and discuss the carry-save multiplier technique.
k) Describe how CPU interacts with peripheral devices.
l) Discuss the role and characteristics of USB interface in I/O systems.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four) **(16 x 2)**

Q3 Describe the architecture, working principle, advantages, and disadvantages of cache memory in detail, including the impact of cache size and block size on performance. **(16)**

Q4 Discuss instruction set architecture of a CPU, including different types of instruction sets, their classifications, and addressing modes with examples. **(16)**

Q5 Consider a cache memory system with the following specifications: **(16)**
Cache size = 64 KB; Block size = 32 bytes; Main memory size = 16 MB
Calculate the following:

I. Number of blocks in cache
II. Number of blocks in main memory
III. Number of tag bits, index bits, and offset bits for a direct-mapped cache
IV. Number of tag bits, index bits, and offset bits for a 4-way set associative cache

Explain each calculation clearly and justify your approach.

Q6 Using floating-point arithmetic, add the following numbers represented in IEEE-754 single-precision format: **(16)**

- Number A = 0 10000001 01000000000000000000000
- Number B = 0 10000000 11000000000000000000000

Clearly illustrate each step: aligning exponents, adding significands, normalization, and final representation.