Registration No: | | | | | | | | | | |

Total Number of Pages: 02 **Course: IDD (B.Tech and M.Tech)/B.Tech**
Sub_Code: EOPC2004

3rd Semester Regular/Back Examination: 2025-26
SUBJECT: Digital Electronics
BRANCH(S): AI, CSE, CSEAI, CSEAIML, CSEDS, CSEIOT, CSIT, CST, IT
Time: 3 Hour
Max Marks: 100
Q.Code : U613

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) What are minterms and maxterms?
b) Find the minimum number of 2-input NAND gates required to implement a 2-input XOR gate.
c) How many OR gate and half adder are required to implement a full adder Circuit?
d) What is essential prime implicant?
e) Perform the following binary arithmetic: (i) 1011 + 0110, (ii) 11100 - 1011
f) Define error-detecting code with an example.
g) Define functional completeness of logic gates.
h) A 4 bit modulo-16 ripple counter uses JK flipflops. If the propagation delay of each Flip-flop is 50 ns. Then find the maximum clock frequency.
i) Find the minimum number of flip-flops required for a Mod-9 (BCD) counter.
j) Define Algorithmic State Machine (ASM).

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Explain SR and JK flip-flops with characteristic tables.
b) Implement the Boolean function F(A, B, C, D) = Σ(1, 3, 5, 7, 8, 12, 14) using a 4-to-1 multiplexer
c) Describe the Quine–McCluskey minimization technique.
d) Explain the working of a serial binary adder.
e) Simplify the Boolean expression F(A, B, C) = A' B' C + A'BC + ABC using a Karnaugh map.
f) Design a 1-bit magnitude comparator using logic gates and extend the concept to a 2-bit comparator.
g) Describe the synthesis of synchronous sequential circuits with an example.
h) Explain flip-flop and design a modulo-N ring counter.
i) Differentiate between decoder and demultiplexer. Under what circumstance a decoder can be converted into demultiplexer?

j) If (1235)x = (3033)y, where x and y indicate the bases of the corresponding numbers, then find the value of x and y.

k) Explain the difference between static and dynamic hazards and describe design techniques to eliminate them

l) A finite state machine is designed using d flip flops. Explain how state assignment impacts power consumption and switching activity in the circuit.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 a) Design of 16×1 MUX using 4×1 MUX. **(8+8)**
b) Convert the SR Flipflop to JK Flipflop.

Q4 a) Design a parity bit generator for a 4-bit data word using logic gates. **(6+10)**
b) Implement a 3-to-8 line decoder using AND and NOT gates. Draw the gate-level realization.

Q5 a) Design a 4-bit sequential adder using shift registers and flip-flops. Explain the gate-level operation. **(8+8)**
b) Design a modulo-6 synchronous counter using T flip-flops. Derive excitation equations and draw the complete gate-level circuit.

Q6 Explain Algorithmic State Machines and discuss system design using ASM for **(8+8)**
c) Weighing machine.
d) Binary multiplier.