Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **Course: B.Tech**

Sub_Code: RBM4C001/REE4C001/REL4C001

4th Semester Back Examination: 2025-26
SUBJECT: Digital Electronics
BRANCH(S): BIOMED, EEE, ELECTRICAL
Time: 3 Hours
Max Marks: 100
Q.Code: S275

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Differentiate between signed and unsigned binary numbers.
b) Perform the following binary arithmetic: (I) 1101 + 1011, (II) 10101 – 1101
c) Convert the decimal number 2455.30 to its binary equivalent.
d) What are error detecting and correcting codes?
e) What is the purpose of the "don't care" condition in Karnaugh maps?
f) What is the function of a priority encoder in digital circuits?
g) Design NAND gate and XOR gate using 2 - input NOR gate.
h) Describe the operation of tri-state logic and its applications
i) Explain the difference between TTL and CMOS logic families.
j) How many flip-flops are required to build a binary counter that counts from 0 to 4095?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Simplify the Boolean expression: (A + B) (A′ + C) (B + C′) using Boolean algebra.
b) Explain the operation of an 8:1 multiplexer. Draw its logic diagram and truth table.
c) Design a JK flip-flop using NAND gates. Explain its operation with a truth table and timing diagram.
d) What is a decoder? Design a 3-to-8 line decoder and explain its operation.
e) Design a 4-bit parallel adder using full adders. Explain its operation and timing diagram.
f) Simplify the Boolean expression F (A, B, C) = A'BC + AB'C + ABC' using a Karnaugh map.
g) What is an Analog-to-Digital Converter (ADC)? Explain the operation of a successive approximation ADC with a block diagram.
h) Design a sample and hold circuit. Explain its operation and applications.
i) What is a ring counter? Design a 4-bit ring counter and explain its operation.
j) Explain the operation of a weighted resistor Digital-to-Analog Converter (DAC).
k) What is a Programmable Logic Array (PLA)? Explain its structure and programming.
l) Discuss the interfacing of CMOS and TTL logic families with suitable examples.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four) **(16 x 2)**

Q3	**a)**	Design a 4-bit binary adder using logic gates.	**(8 + 8)**
	b)	Implement an XOR gate using only NAND gates.	
Q4	**a)**	Implement the Boolean function F (A, B, C, D) = Σ (0, 1, 2, 4, 8, 9, 15) using a 4-to-1 multiplexer.	**(8 + 8)**
	b)	Define sequential circuits. Explain the operation of a clocked SR flip-flop with its truth table and timing diagram	
Q5	**a)**	What is a shift register? Design a 4-bit serial-in serial-out (SISO) shift register and explain its operation.	**(8 + 8)**
	b)	Explain the operation of a 4-bit ripple counter. Draw its logic diagram and timing diagram.	
Q6	**a)**	Define Field Programmable Gate Array (FPGA). Discuss its architecture and applications	**(8 + 8)**
	b)	Explain the concept of charge-coupled device (CCD) memory. Discuss its advantages and disadvantages.	