Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **Course: IDD (B.Tech and M.Tech)**
Sub_Code: EOPC2006

4th Semester Regular Examination: 2024-25
SUBJECT: Digital Systems Design
BRANCH(S): AEIE, ECE, EEVDT, ETC, ECE
Time: 3 Hours
Max Marks: 100
Q.Code: S335

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Write '–5' in signed 1's complement, signed 2's complement and signed magnitude form.
b) X = 1010100 and Y = 1000011, perform the subtraction Y – X by using 2's complements.
c) The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are x = 3 and x = 6. What is the base of the numbers?
d) Define the term "digital signal" and give two examples.
e) Find the complement of the function F = X (Y'Z' + YZ) by taking their duals and complementing each literal.
f) Simplify the Boolean function F (x, y, z) = ∑ (2, 3, 4, 5)
g) What is the main advantage of using a carry-look ahead adder over a ripple-carry adder?
h) What is the difference between Synchronous Counter and Asynchronous Counter?
i) Define the characteristics of digital ICs.
j) What is the purpose of the capacitor in a DTL circuit?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Obtain the truth table of the Boolean function (A' + B) (B' + C) and express each function in sum of min terms and product of maxterms.
b) State and prove De Morgan's laws.
c) Simplify the Boolean function F (A, B, C, D) = ∑ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) using four variable K-map.
d) Define combinational logic circuits. Design a half-adder using NAND gates and NOR gates
e) Explain the operation of a 4- Bit by 3-Bit binary multiplier.
f) Discuss the applications of multiplexers and demultiplexers in digital systems.
g) Explain the operation of a 3-line to 8-line decoder with a truth table.
h) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.
i) Discuss the working of a 4-bit magnitude comparator and its applications

j) What is a shift register? Design a four-bit shift register using D flip-flop and explain its operation.

k) Design a 4-bit parallel adder using full adders. Explain its operation and timing diagram.

l) Explain the concept of charge-coupled device (CCD) memory.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four) **(16 x 2)**

Q3 **a)** Explain Mealy and Moore models of Finite State Machine with suitable block diagram. **(8 + 8)**

b) Implement the Boolean function F (A, B, C, D) = ∑ (0, 2, 5, 7, 11, 14) with a multiplexer.

Q4 **a)** A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 Seconds. YELLOW is turned on for 5 Seconds and the RED is turned on for 75 seconds. The traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock of 5 second period. Implement this FSM using minimum number of flip-flops. **(8 + 8)**

b) Design a one input, one output serial 2's complementer. The circuit accepts a string of bits from the input and generates 2's complements at the output. The circuit can be reset asynchronously to start and end the operation

Q5 **a)** Draw the logic diagram of a four-bit binary ripple countdown counter using flip-flops that trigger on the positive edge of the clock. **(8 + 8)**

b) Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6 (Use D flip - flop)

Q6 **a)** Discuss the characteristics of TTL and CMOS logic families, highlighting their differences. **(8 + 8)**

b) What is a Programmable Logic Array (PLA)? Explain its structure and programming.