Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
REC5D006

5th/7th Semester Reg/Back Examination: 2025-26
SUBJECT: Digital VLSI Design
BRANCH(S): AEIE, CSE, ECE, EEE, ELECTRICAL, ETC, IT, MECH
Time : 3 Hour
Max Marks : 100
Q. Code : U413

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) What is CMOS n-well process?
b) What is meant by dynamic logic?
c) If the mobility of NMOS is 450 cm²/V-s, gate width 10 µm, length 2 µm, Cox = 4 fF/µm², and V_{GS} = 3V, V_{th} = 0.8V, compute Id (saturation).
d) Write and explain the expression for dynamic power consumption.
e) What is bootstrapping in MOS circuits?
f) What is IDDQ testing?
g) For CMOS inverter with supply V_{DD} = 5V and switching threshold V_m = 2.5V, find noise margin (NMH, NML).
h) A DRAM cell stores charge Q = 45 fC at V = 1V. Compute storage capacitance.
i) CMOS inverter switching energy is 1.6 pJ per transition. Compute power at f = 200 MHz.
j) Define MOSFET scaling.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Explain stuck-at fault model with examples for s-a-0 and s-a-1 in a logic line.
b) Explain how interconnect parasitic affect switching delay in VLSI systems.
c) Explain stick diagrams and draw stick diagram for CMOS inverter.
d) Write detailed note on CMOS layout design, masks, and λ-based design rules.
e) Design CMOS logic circuits for following functions:
(I) Y = A+B' (II) Y = AB + C
f) Discuss BIST architecture and its types
g) Describe working principle and structure of 6T SRAM cell.
h) A CMOS inverter has load capacitance = 50 pF and R = 8 kΩ. Calculate rise time, fall time, and propagation delay.
i) Describe the various steps involved in CMOS n-well fabrication process.
j) Explain Built-In-Self-Test (BIST) architecture with MISR and LFSR block diagram.
k) Explain operation of 6-T SRAM with neat circuit diagram & timing waveform.

I) Explain stability analysis of SRAM cell using butterfly curves.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3	**(a)**	Derive the delay time expressions for CMOS inverter and discuss design for minimum delay	**(10)**
	(b)	Explain estimation of interconnect delay in MOS circuits with examples	**(6)**
Q4	**(a)**	Describe dynamic logic circuits in detail with operation, structure and timing issues.	**(10)**
	(b)	Discuss high-performance dynamic CMOS circuits.	**(6)**
Q5	**(a)**	Compare DRAM, SRAM and Flash memory based on structure, speed, power and applications.	**(10)**
	(b)	Explain non-volatile memory organization with diagrams.	**(6)**
Q6		A CMOS inverter drives a load of CL = 120 fF. PMOS width = 3 μm, NMOS width = 1 μm, μp = 150 cm²/V-s, μn = 450 cm²/V-s	**(16)**
	(a)	Compute propagation delay.	
	(b)	Estimate dynamic power at 100 MHz, VDD=1.8V.	