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Total Number of Pages : 02

B.Tech/ Integrated Dual Degree  
RCS4C003

4<sup>th</sup> Semester Reg/Back Examination: 2023-24

Computer Organization and Architecture

CSE, CSEAI, CSEAIME, CSEDS, CST, IT

Time : 3 Hour

Max Marks : 100

Q. Code : P394

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions: (2 x 10)

- Mention the difference between Computer Organization and Computer Architecture
- Mention the difference between big-endian and little-endian representations.
- What is an instruction format? Explain the fields in the instruction format.
- Represent  $+1.7$  using IEEE 754 single precision and double precision format.
- Explain the difference between main memory and control memory.
- Enlist the types of registers used in a microprocessor.
- Define the following terms: *memory access time*, *memory cycle time*.
- List out the disadvantages of DRAM over SRAM.
- Define instruction stream and data stream. Give an example of SISD computer system.
- Define an interrupt. Differentiate between software and hardware interrupts.

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- Discuss the instruction execution cycle elaborating about different types of registers used
- Design a 4-bit carry look ahead adder with clear expressions for Propagate and Generate functions. Also draw the circuit diagram.
- Briefly explain the two hardware methods to establish priority.
- Compute the number of cycles required to execute 100 tasks in a 5 stage pipeline system. Derive the speed-up ratio and determine the time required to execute the same 100 tasks in a non-pipeline processor.
- A block set-associative cache consists of 64 blocks divided into 4 block-sets. The main memory contains 4096 blocks, each consisting of 128 words. How many bits are there in a main memory address? How many bits are there in each of the TAG, SET and WORD fields?
- Perform the division of 10 by 7 by using restoration method.
- Explain about the micro-sequencer unit with a neat diagram.

- h) Write the following expression using three-address, two address and one-address format:  $A+B/(D*E)-F$
- i) Explain about the virtual memory concept. Why is it required? Explain about the page table and the TLB.
- j) What is RTL? Describe various methods of RTL. List the basic symbols and its use in RTL.
- k) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the no 200. Evaluate the Effective Address if the addressing mode of the instruction is :
- Direct
  - Immediate
  - Relative
  - register Indirect
  - Index with R1 as the Index Register
- l) The memory unit of a computer has 512K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of the eight addressing modes, a register address field to specify one of the 70 processor registers and a memory address. Specify the instruction format and the number of bits in each field.

### Part-III

#### Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** What do you mean by an addressing mode? Explain the importance of different addressing modes in computer architecture with an example from each. **(16)**
- Q4** Explain Booth's algorithm with the help of a flowchart. Multiply  $(-3)_{10}$  with  $(8)_{10}$  using Booth's algorithm. Highlight the demerits of Booth's algorithm for which modified Booth's algorithm is used. **(16)**
- Q5** What is the importance of Direct Memory Access? Explain the working of DMA Controller with a neat diagram. **(16)**
- Q6** What is pipelining? What are the hazards that are encountered in a pipeline system? Given below the code, identify the hazards and explain the solution to those: **(16)**
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ADD R1,R2,R3
SUB R2,R4,R6
XOR R3,R1,R2
OR R3,R4,R5

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