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Total Number of Pages : 02

B.Tech
RCS4C003/ RIT4C003

4th Semester Regular/ Back Examination: 2022-23
SUBJECT: Computer Organization and Architecture
BRANCH(S): CST,CSEAI,CSE,CSEAIME ,IT

Time : 3 Hour
Max Marks : 100

Q.Code : M261

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions:

(2 x 10)

- Draw the basic functional units of a computer.
- Write down the operation of control unit.
- List out the various addressing techniques.
- Calculate the following: Add 5_{10} to 6_{10} in binary and subtract -6_{10} from 7_{10} in binary.
- What is underflow in floating point arithmetic?
- Divide $(12)_{10}$ by $(3)_{10}$
- Discuss the principal operation of micro programmed control unit.
- What is I/O control method?
- Define hazard. Give an example for data hazard.
- Evaluate hit ratio and effective access times in cache.

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 × 8)

- Explain instruction set Architecture. Give examples.
- Explain in detail about different instruction types and instruction sequencing.
- What is RTL? Describe various methods of RTL. List the basic symbols and its use in RTL.
- List the steps of multiplication algorithm.
- State the purpose of Look Ahead Carry Adder. Derive the expressions for propagate and generate functions of a 4-bit Look Ahead Carry Adder and draw its schematic.
- Examine with a neat block diagram how floating point addition is carried out in a computer system.
- Give comparison between memory mapped I/O and I/O mapped I/O.
- Describe the working principle of USB.
- Describe hyper-threading.

- j) Design and develop an instruction pipeline working under various situations of pipeline stall.
- k) Mention the need for cache memory. Explain the following three mapping methods with examples.
- i) Direct
 - ii) Associative
 - iii) Set associative
- l) What is hardware multi-threading? Explain different types of multi-threading occurs in parallel architectures.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** What is zero address instruction format? Give an example. Enumerate the most commonly used addressing modes of CPU instructions. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. what is the effective address of the memory operand of the following instruction:
Load 25(R1), R5. **(16)**
- Q4** Write down the Booth's algorithm. List the two attractive features of Booth's algorithm. Give an example for worst case of Booth's algorithm. **(16)**
- Q5** Summarize the virtual memory organization followed in digital computers. **(16)**
- Q6** Assume the following sequence of instructions are executed on a 5 stage pipelined processor
Or r1, r2, r3
Or r2, r1, r4
Or r1, r1, r2 **(16)**
- i) Indicate dependences and their type.
 - ii) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them.
 - iii) Assume there is a full forwarding. Indicate hazard and add NOP instructions to eliminate them.