Registration No :

4th Semester Regular/Back Examination: 2023
SUBJECT: Digital Electronics
BRANCH(S): BIOMED, EEE, ELECTRICAL
Time : 3 Hour
Max Marks : 100
Q.Code : M217
Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Write the binary equivalent of $(101.11)_8$

b) What is the importance of Priority encoder?

c) Draw CMOS logic circuit & write its one application.

d) What is the specialty of EX-OR gate?

e) Compare synchronous counter with asynchronous counter.

f) What is the minimum number of flip-flops needed to design a mod-16 counter?

g) Define PLA & PAL.

h) Write some applications of MUX & DMUX.

i) How JK Flipflop is converted to T-Flipflop?

j) What is FPGA?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Draw TTL circuit & explain its operation.

b) Draw the truth table & circuit for full Adder. Also mention its output equations.

c) Implement the given functions using single 3:8 decoder.

$$f_1(A,B,C) = \prod(2,3,4,5,7)$$

$$f_2(A,B,C) = \sum(1,3,5)$$

d) Do a conversion of SR-FF to D-FF with detailed truth table & K-Map analysis.

e) Discuss any two error detecting codes & also any two correcting codes with examples.

f) Design a 2-bit synchronous up counter.

g) Write down two applications of each for MUX, Flipflop, Counter, Ex-OR gate, shift register & CMOS.

h) Simplify the expression using K-maps: $F(x, y, z) = \pi(0,2,4,5,7)$

i) Explain operation of ring counter with suitable output wave diagram.

j) The initial contents of the 4-bit serial in parallel out shift register is 1011. What will be contents of the given shift register after 5 clock pulses applied?

k) Explain operation of successive approximation A/D converter.

l) Draw a ROM structure & discuss its function.

Part-III
Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** Discuss operation of the carry look ahead adder with the proper logic flows. **(8)**

b) Obtain the simplified form for the given expression using K-map. **(8)**

Also, draw the minimization result using NAND gate only.

$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$

Q4 **a)** A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3 input majority circuit. **(8)**

b) Find the Boolean function for 8:1 MUX. **(8)**

Q5 **a)** Design a decade counter by using JK-FF or T-FF. **(8)**

b) Explain shifting of data in serial left & serial right manner with suitable logic circuits. **(8)**

Q6 **a)** How analog to digital conversion happens, Show it stepwise. **(8)**

b) Explain PLD & CPLD. **(8)**