Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **Integrated Dual Degree (B.Tech and M.Tech)**
REC4C002/RME4G001/REI4C002

4th Semester Regular/Back Examination: 2023-24
SUBJECT: Digital Systems Design
BRANCH(S): ECE,ELECTRONICS & CE,ETC,MECH,MMEAM,AEIE,EIE
Time: 3 Hour
Max Marks: 100
Q.Code: P313
Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Convert $(5064)_9$ into base 5.
b) Show that A+B. C = (A+B).(A+C)
c) What is the importance of parity bit?
d) State the need for a tristate buffer.
e) How race condition in JK flipflop can be resolved?
f) Differentiate between level clocking and edge triggering.
g) List the advantages of CMOS.
h) What problem could occur when the counter circuit is powered-up?
i) Write any three differences between EEPROM and UVEPROM.
j) Define access time and word length of a memory chip.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Perform the arithmetic operation (+42) + (–13) and (–42) – (–13) in binary using the signed 2's-complement representation for negative numbers.
b) Consider a 4-input Boolean function that outputs a binary 1 whenever an odd number of its inputs are binary 1.Using Boolean logic or otherwise, show how the above function can be implemented using only 2-input XOR gates.
c) How parity checkers help in finding errors in digital data transmission?
d) What is associative memory? Draw and explain its block diagram.
e) Find the POS for the function F(x, y, z) = π (0, 1, 4, 5).
f) Design a BCD to decimal decoder.
g) Design a 5 x 32 decoder with four 3 x 8 decoder with enable and one 2 x 4 decoder. Use block diagrams only.

h) A sequential circuit with 2 JK Flip Flops A and B, two inputs X and Y, and one output Z. The Flip Flop input equations and circuit output equations are
$J_A = B'Y'+BX$, $K_A = B'XY'$, $J_B = A'X$, $K_B = A+XY'$ and $Z = AX'Y'+ BX'Y$
Draw the logic diagram of the circuit with the state table.

i) With the aid of block and example state diagrams, describe the main features of Moore and Mealy implementations of finite state machines.

j) What is asynchronous counter? Design asynchronous counter that counts the sequence of 0-1-4-6-7 using T flip-flop.

k) Explain the working of R-2R ladder type DAC.

l) Implement a 4:1 MUX circuit using VHDL.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** Prove that a positive-logic AND gate is a negative-logic OR gate and vice-versa. **(4)**

b) Apriority encoder has 2N inputs. It produces an N-bit binary output indicating the most significant bit of the input that is TRUE, or 0 if none of the inputs is TRUE. It also produces an output NONE that is TRUE if none of the inputs is TRUE. **(12)**

(i) Write down the Truth table showing all inputs and all outputs for an eight-input priority encoder.

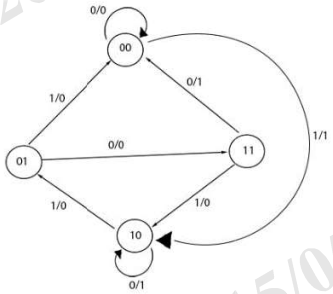
(ii) Give simplified Boolean expressions for all outputs of the eight-input priority encoder.

Q4 **a)** Design a combinational circuit with three inputs and six outputs. The output binary number should be the square of the input binary number. **(8)**

b) Draw a neat diagram of TTL NAND gate and explain its operation. What is meant by sourcing and sinking? **(8)**

Q5 **a)** Draw the block diagram of a 4 bit ALU, and explain it, showing its inputs and outputs. **(6)**

b) **(10)**



Design the sequential circuit with respect to the above state diagram using J-K flip flops.

Q6 **a)** Implement the circuit of a PLA with 3 input, 2 output, and 4 product terms **(8)**
$F_1(A, B, C) = \sum (3,5,6,7)$, $F_2(A, B, C) = \sum (0,2,4)$

b) What is the difference between a serial and a parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed? **(8)**