Registration No :

4th Semester Regular/ Back Examination: 2022-23
SUBJECT: Digital Systems Design
BRANCH(S): ECE, ELECTRONICS & C.E, ETC, AEIE, EIE, MMEAM, MECH
Time : 3 Hour
Max Marks: 100
Q.Code : M160
Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1   **Answer the following questions:**   (2 x 10)

a) Differentiate between Analog and Digital system. What are the advantages of a digital system?

b) Using 2's complement perform subtraction (1000100 – 1010100).

c) Define integrated circuit. What are the characteristics that describe the performance of IC digital logic families?

d) Explain why NAND-NAND realization is preferred over AND-OR realization?

e) When did the first PLD appear?

f) What are gate primitives?

g) What are Fan-in and Fan-out?

h) The initial state of MOD-16 down counter is 0110. What state will it be after 37 clock pulses?

i) In a positive edge triggered JK flip flop, J = 1, K = 0 and clock pulse is rising Q will be _____.

j) Which are the basic refresh modes for dynamic RAM?

Part-II

Q2   **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)**   (6 × 8)

a) Explain parity generator and checker with suitable example.

b) Design a half adder using at most three NOR gates.

c) Describe the read and write cycle of a DRAM. Also describe about the fast page mode.

d) Design a combinational circuit that accepts a three-bit binary number and generates an output binary number equal to the square of the input number.

e) Calculate analog output of 4-bit DAC for digital input 1011. Assume V_{FS} = 5V.

f) Design a counter with the following binary sequence: 0, 4, 2, 1, 6 and repeat. Use JK flip-flops.

g) With an example explain in detail the test bench creation.

h) Discuss the TTL parameters. Draw the TTL inverter circuit.

i) Design a MOD-10 synchronous counter using T flip flops.

j) Compare TTL and CMOS logic families based on following:
(a) Propagation delay (b) Power dissipation

k) Briefly explain the pulse mode asynchronous sequential circuit.

l) Explain the different methods of state assignment.

Part-III
Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 **(a)** Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit. **(08)**

(b) Draw and explain logic diagram of arithmetic logic unit (ALU). **(08)**

Q4 **(a)** Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions: **(09)**
$F1 = x'y'z + xz'$
$F2 = x'yz' + xy'$
$F3 = xyz' + xy$

(b) Explain various steps in the analysis of synchronous sequential circuits with suitable example. **(07)**

Q5 **(a)** Design a 4-bit synchronous 8421-decade counter with ripple carry. **(08)**

(b) With respect to Register Transfer logic, explain Inter register transfer with necessary diagrams. **(08)**

Q6 **(a)** Write VHDL program for 4:1 MUX using behavioral modeling. **(10)**

(b) Explain PLA with necessary diagrams. **(06)**